AFRL-IF-RS-TR-2001-205
Final Technical Report
October 2001

COMPUTER-AIDED DESIGN (CAD) TOOLS FOR AN INTEGRATED MILLIMETER WAVE WIRELESS COMMUNICATION MICROSYSTEM

University of Illinois at Urbana - Champaign

Sponsored by
Defense Advanced Research Projects Agency
DARPA Order No. E117

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

AIR FORCE RESEARCH LABORATORY
INFORMATION DIRECTORATE
ROME RESEARCH SITE
ROME, NEW YORK

This report has been reviewed by the Air Force Research Laboratory, Information Directorate, Public Affairs Office (IFOIPA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

AFRL-IF-RS-TR-2001-205 has been reviewed and is approved for publication.

APPROVED: 

DAVID C. WILLIAMSON
Project Engineer

FOR THE DIRECTOR: 

MICHAEL L. TALBERT, Technical Advisor
Information Technology Division
Information Directorate

If your address has changed or if you wish to be removed from the Air Force Research Laboratory Rome Research Site mailing list, or if the addressee is no longer employed by your organization, please notify AFRL/IFTC, 26 Electronic Pky, Rome, NY 13441-4514. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

COMPUTER-AIDED DESIGN TOOLS FOR AN INTEGRATED MILLIMETER WAVE WIRELESS COMMUNICATION MICROSYSTEM

Chang Liu

Contractor: University of Illinois at Urbana - Champaign
Contract Number: F30602-97-2-0328
Effective Date of Contract: 28 August 1997
Contract Expiration Date: 28 August 2000
Short Title of Work: CAD Tools for an Integrated Millimeter Wave Wireless Communication Microsystem
Period of Work Covered: Aug 97 - Aug 00

Principal Investigator: Chang Liu
Phone: (217) 333-4051
AFRL Project Engineer: David C. Williamson
Phone: (315) 330-7324

This research was supported by the Defense Advanced Research Projects Agency of the Department of Defense and was monitored by David C. Williamson, AFRL/IFTC, 26 Electronic Pky, Rome, NY.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	OCTOBER 2001	Final Aug 97 - Aug 00

4. TITLE AND SUBTITLE
COMPUTER-AIDED DESIGN (CAD) TOOLS FOR AN INTEGRATED MILLIMETER WAVE WIRELESS COMMUNICATION MICROSYSTEM

5. FUNDING NUMBERS
C - F30602-97-2-0328
PE - 63739E
PR - E117
TA - 00
WU - 26

6. AUTHOR(S)
Chang Liu

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
University of Illinois at Urbana - Champaign
313 Microelectronics Laboratory
208 North Wright Street
Urbana Illinois 61801

8. PERFORMING ORGANIZATION REPORT NUMBER
N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Defense Advanced Research Projects Agency
3701 North Fairfax Drive
Arlington VA 22203-1714

Air Force Research Laboratory/IFTC
26 Electronic Pky
Rome New York 13441-4514

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
AFRL-IF-RS-TR-2001-205

11. SUPPLEMENTARY NOTES
Air Force Research Laboratory Project Engineer: David C. Williamson/IFTC/(315) 330-7324

12a. DISTRIBUTION AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The central objective of this three-year composite CAD project titled "CAD Design Tools for an Integrated Millimeter Wave Wireless Communication Microsystem" is to develop efficient and accurate computer simulation algorithms and algorithms for analysis of mixed-technology communication systems consisting of both circuits and micro electromechanical systems (MEMS). In addition, we conducted research on the development of prototype devices in order to validate the simulation software and to demonstrate the capabilities of the simulation tools.

In this report, we discuss the major work accomplished in this project under six categories: 1) Advanced simulation of electromagnetic fields; 2) Mixed technology circuit level simulation; 3) Design of low voltage radio frequency switches; 4) Development of ACES (Anisotropic crystalline etching simulation); 5) Simulation of RF packages and interconnects; and 6) Development of integrated RFIC passive components.

14. SUBJECT TERMS
Computer-Aided Design Tools, CAD, Millimeter Wave, Wireless Communication, Microelectromechanical Systems, MEMS

15. NUMBER OF PAGES
40

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Table of Contents

List of Figures

List of Tables

1. Summary

The central objective of this three-year composite CAD project titled "CAD Design Tools for an Integrated Millimeter Wave Wireless Communication Microsystem" is to develop efficient and accurate computer simulation algorithms and algorithms for analysis of mixed-technology communication systems consisting of both circuits and micro electromechanical systems (MEMS). In addition, we conducted research on the development of prototype devices in order to validate the simulation software and to demonstrate the capabilities of the simulation tools.

The objectives of the project have been successfully met through the collaborative research of five faculty members on the campus of the University of Illinois. These faculty members and their expertise areas include: (1) Prof. Chang Liu, principal investigator, MEMS design and development, (2) Prof. Steve Kang, mixed-technology circuit simulation using reduced-order algorithms, (3) Prof. Milton Feng, high frequency communication chips, (4) Prof. Jose Schutt-Aine, circuit parameter extraction of complex three-dimensional geometry, (5) Prof. Eric Michielssen, fast simulation algorithms for electromagnetic radiation.

In this report, we discuss the major work accomplished in this project under five categories:

(1) Advanced simulation of electromagnetic fields;
(2) Mixed technology circuit level simulation;
(3) Design of low voltage radio frequency switches;
(4) Development of ACES (Anisotropic crystalline etching simulation);
(5) Simulation of RF packages and interconnects;
(6) Development of integrated RFIC passive components.

2. Introduction

This three-year program coincides with the explosive growth of radio frequency MEMS (RF MEMS). RF MEMS components that have been developed recently include micromechanical resonators, band-pass filters, integrated tunable capacitors, integrated inductors, micro antennas, micro relays and switches, and precision MEMS packages made by micromachining processes.

Certain MEMS components offer advanced performances compared with conventional circuit counterparts. For example, microfabricated mechanical switches offer low insertion loss and high rejection over conventional transistor- or diode-based switches. Such advantage is important in RF applications including arrayed antennas.

MEMS RF components are also important for realizing integrated RF systems-on-a-chip. Traditionally it is difficult to integrated discrete components such as capacitors, resonators, and inductors on a single chip along with the transistor circuits. This increases the costs of RF systems by increasing the complexity of packaging. MEMS offers unique solutions for integrating capacitors, inductors and resonators on chip using compatible fabrication processes.

However, the design of such systems is made difficult by the low speed and high cost of simulation. Software that exists at the start of the project was not capable of efficient and comprehensive simulation of (1) radiation from highly complex three-dimensional geometries; and (2) mixed-technology circuit-MEMS systems. Our project was therefore motivated by the need of advancing the state-of-the-art of RF system design.

There are four major tasks in this effort.
(1) Task 1: CAD tools for integrated antennas:
(2) Task 2: CAD tools for MEMS switches and interconnects;
(3) Task 3: Scalable MMIC module with MEMS components;
(4) Task 4: Design flow management and technology transfer.

3. Results and Discussion

3.1. Advanced Simulation of Electromagnetic Radiation

3.1.1. Frequency domain simulation tools

In the first year of the program we focused on the development of fast frequency-domain simulation tools. We have developed computational codes that adopt the Steepest-Descent Fast Multipole Method (SDFMM) with the Method of Moment (MOM), based on preliminary algorithms and coded developed by former members of Erik Michielssen's group. New codes will allow three-dimensional solid models (Fig. 1) to be effectively incorporated.

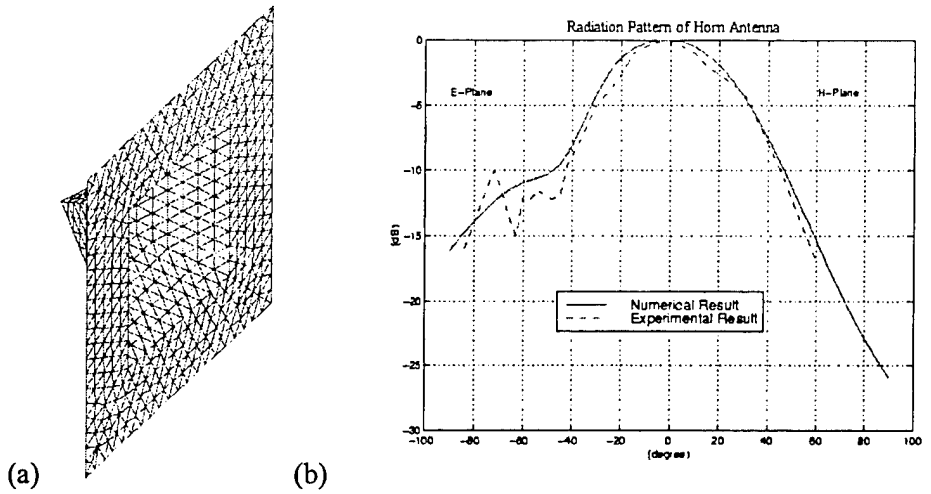


Figure 1: (a) Meshed model of a micromachined horn antenna; (b) spatial distribution of RF radiation simulated using the frequency-domain simulation tools.

The simulation tools allow us to explore new antenna designs and minimize time spent on trial-and-error prototyping. We have also used the frequency-domain simulation tools in designing highly complex reconfigurable antenna geometries such as the log-periodic slot array (LPSA) antenna shown in the diagram below (Fig. 2). These designs have added functionality when compared to conventional models. The LPSA antenna comprises an extension of a dual-mode LPSA in the sense that more than two LPSAs are combined together so that the radiation pattern may cover the entire azimuthal plane. By using RF switching (e.g. MEMS switches), the radiation beam may be steered in both azimuth and elevation. Compared with the previous designs, this antenna is easily reconfigured and general-purpose. This design takes advantage of two sets of MEMS switches to configure the antenna backplane and radiation plane.

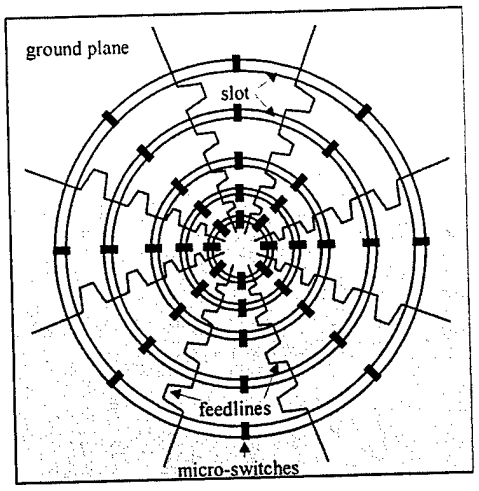


Figure 2: Schematic diagram of a reconfigurable LPSA antenna.

3.1.2. Time domain simulation tools

Following the successful development of frequency-domain simulation, we have developed the full multi-level two-dimensional plane wave time domain (2D PWTD) algorithm. Our central objective is to enable fast transient electromagnetic field solver that can solve within a matter of minutes complex microwave and millimeter wave devices including MEMS devices. Such devices would contain multiple conducting and insulating layers, reside in a lossy substrate, and contain finely meshed geometric details. Time domain algorithms are desired for simulation of transient behavior. In this area, the major contribution of this program is the developed of fast algorithms for time domain simulators.

In order to estimate the distribution of electromagnetic field around an arbitrary object (Fig. 3), it is necessary to solve the discrete matrix form representation of the Maxwell's equations. The PWTD algorithm reduces the computational complexity significantly. Assume that there are Ns spatial and Nt temporal unknowns, the complexity of two-dimensional evaluation is reduced from $O(N_tN_s^2)$ to $O(N_tN_sLog^2N_s)$.

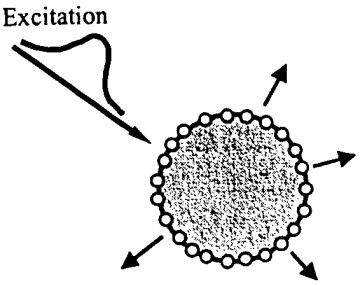


Figure 3: Schematic diagram of incoming wave to a scattering object.

Our approach was to extend PWTD algorithms to accommodate MEMS features. Specifically, we developed the following extension kernels listed below.

1. –PWTD kernels for layered media

2. –PWTD kernels for low frequency problems
3. –PWTD kernels for nonlinear phenomena
4. –PWTD kernels for penetrable objects
5. –PWTD kernels for lossy media
6. –PWTD kernels coupled to higher order solvers

As an example, one challenge facing the application of PWTD to layered structures lies in the fact that Green functions in layered media have long tail, leading to increased computational complexity. We have developed a new technique of PWTD in conjunction with Hilbert transform. The computational complexity is reduced from $O(N_t^2 N_s^2)$ to $O(N_t \mathrm{Log} N_t N_s \mathrm{Log}^2 N_s)$.

Traditional TDIE and PWTD schemes break down at low frequencies, or when portions of the structure being simulated is very finely meshed. We have developed new TDIE schemes that are stable all the way down to DC. These schemes are based on loop-star (Helmholtz) decompositions of the currents (Fig. 4). We have developed PWTD schemes that are efficient all the way down to DC. These schemes constitute low frequency extensions of our high frequency methods.

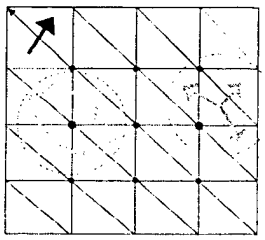


Figure 4: Schematic diagram of the loop-star decomposition of currents.

We applied the 2D PWTD scheme to accelerate the evaluation of low-frequency, finite difference time domain boundary kernels, i.e., to construct global and fast boundary conditions that do not pose a serious computational bottleneck. This hybrid method is especially suitable for the analysis of large complex inhomogeneous problems. Simulation results of voltage and current distribution on an antenna feed line (Fig. 5a) is shown in Fig. 5b. The time history of voltage at two points of interests are illustrated on Fig. 5c.

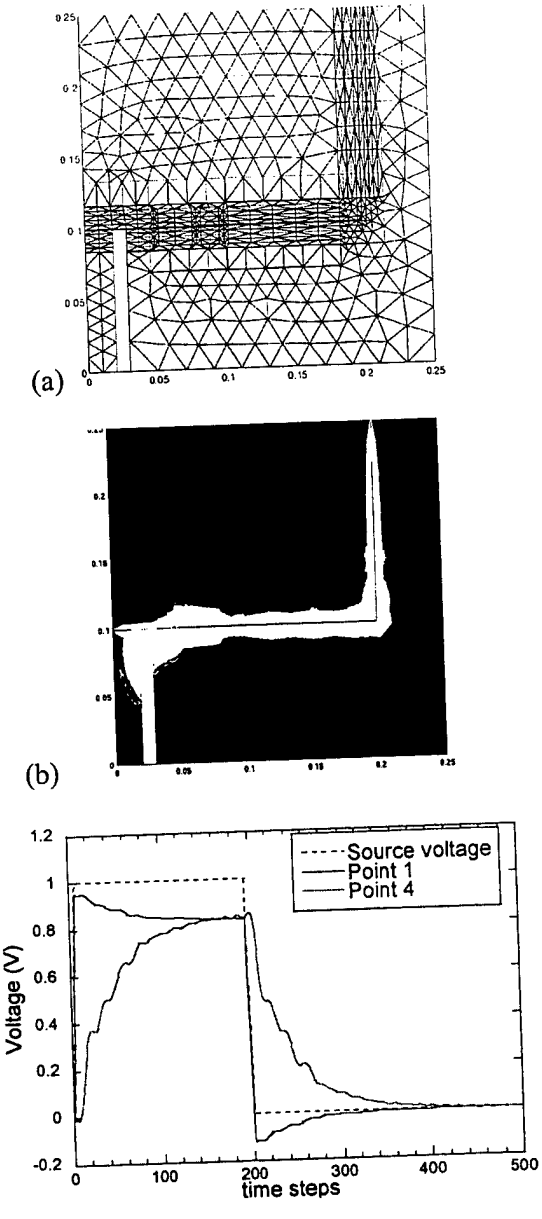


Figure 5: Simulation results of EM distribution near a micro antenna. (a) Meshed model; (b) instaneous current distribution; (c) temporal distribution of voltage.

3.2. Mixed Technology Circuit Level Simulation

Developing of accurate, easy-to-use, fast dynamic macro-model of MEM devices is a difficult and critical task in the MEMS research community. When MEMS devices are embedded in a complex system, designers need fast and accurate dynamic models that permit rapid simulation of system performance under a variety of inputs and scenarios, such as being inserted into a feedback loop. And since direct simulation of 3D structures involves thousands of degrees of freedom and different energy domain forces coupled together, fully nonlinear dynamic simulation becomes computationally infeasible in a typical workstation environment. Furthermore, designers tend to think in terms of models with only a few degrees of freedom that are well correlated to modifiable parameters like dimensions or material properties. Therefore, finding

robust methods to project the results of detailed MEM device-level simulation together with their numerous degrees of freedom onto space spanned by a very small number of variables (called a nonlinear dynamic macro-modeling) is very essential.

The integration of micro-mechanical structures with electronics has increased the demand for new CAD tools to support rapid design and simulation of systems involving physical interactions between mechanical domain and circuit domain. To meet such demand, an open-ended and expandable simulation framework, iSIMS simulator, has been developed. As an integrated piece of software, iSIMS enables transient simulation of entire micro-electro-mechanical systems in a fast and efficient manner. To overcome the shortcomings of conventional finite element based direct numerical dynamic simulation, reduced order MEMS device models have been developed and used for fast and accurate simulation. This greatly reduces the simulation time. Novel techniques for automatically generating reduced-order dynamic models for coupled-domain nonlinear MEMS devices are invented. Techniques for electrical modeling of MEMS device are developed. Event-driven simulation methodology for composite circuit and micro-mechanical simulation is also developed and implemented.

At present, composite simulation is most often performed by coupling the finite element field solver ANSYS with the SPICE circuit simulator. Such coupling of SPICE and finite element simulation is computationally expensive as transient analysis of micromechanical device must be performed by the field solver using fully meshed structures. Convergence may also be a problem in such simulations since the two simulators are not inherently coupled and require iterations between them. Another approach is to treat MEMS devices as lumped parameter elements that are modeled by system of differential and algebraic equations (DAEs). Behavioral modeling languages (e.g. MAST and VHDL-AMS) are then used to allow parameterized MEMS device DAE models to be co-simulated with circuit components in system-level simulators such as SABER and Eldo simulators. This approach enables a structured representation for fast top-down design of suspended micro-electro-mechanical systems using a hierarchical set of MEM components. However, it provides low accuracy due to its rigid body assumption and linear approximations. Many MEMS devices with beam and membrane structures cannot be accurately modeled as lumped elements.

To overcome the shortcomings of the these approaches, the iSIMS simulator combines novel model-order reduction algorithms for automatically generating accurate reduced-order MEMS device models with advanced simulation techniques for fast and efficient simulation of MEMS. The overall architecture of the software is shown at Fig. 6.

Specifically, Taylor series expansion with Arnoldi method is developed for model-order reduction of weakly nonlinear MEMS devices and Karhunen-Loeve Galerkin's method is developed for model-order reduction of strongly nonlinear MEMS devices (please refer to last QSR for details). With the development of reduced MEMS device models, we can perform fast and accurate composite simulation. The following figure illustrates the iSIMS simulator architecture. The iSIMS software provides a general event-processing and scheduling framework that ties together various simulation algorithms needed for simulation of composite circuit and micro-mechanical systems. An iterative timing analysis (ITA) is a relaxation-based algorithm for electrical and functional level simulation. The models associated with it include transistors, capacitors, inductors, resistors and controlled sources. Logic algorithm processes behavioral descriptions of logic gates. Currently, the simulator includes over 40 models for logic gates. Analog Behavioral algorithm handles both s-domain transfer functions and differential equations. User-defined algorithm is to process any user defined high-level mathematics functions. The reduced-order MEM device models represented by the small set of nonlinear ODEs are solved

using this algorithm. Event-driven, selective trace techniques are used for simulation. Matrix representation and single time-step are not required.

Most semiconductor sensors convert the physical parameter being measured into either resistance change or capacitance. To perform composite electrical and mechanical simulation, MEMS device reduced models must include both mechanical part (calculation of device deformation and thus the resistance or capacitance) and electrical part (stamped variable resistor or variable capacitor models). Also the stamps and right half side (RHS) of the electrical variable resistor or capacitor models need to be updated at every time point. In the figure below, the flow diagram for electrical modeling of MEMS devices is presented.

We have applied the algorithms for simulation of various devices. One example is a capacitive pressure sensor system (Fig. 7) where the capacitive sensor is modeled by coupling the forth-order mechanical plate equation and the squeeze-film damping equation. The sensor capacitance C_p is pumped against a reference capacitor C_r, to which it is normally matched. During pressure measurement, the difference charge, which is proportional to C_p-C_r is integrated to produce a voltage output which can be physically measured. During the simulation, a harmonic pressure input is assumed. Simulation result by iSIMS is also given. The inputs to the simulator are the pressure sensor geometry and material parameters. Also users need to specify the netlist of the sensor system just like running the SPICE simulator.

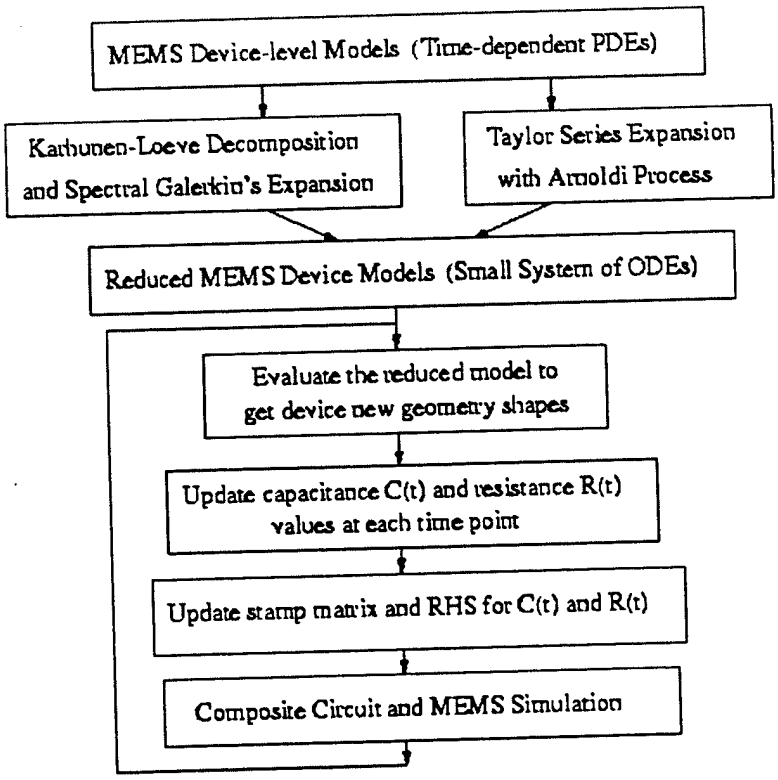


Figure 6: Schematic diagram of the iSims simulator.

Using the iSIMS software we have also designed and simulated the performance of a voltage controlled oscillator (Fig. 8a) that contains micromechanical capacitors. The VCO device has been fabricated using IC foundry process (Fig. 8b).

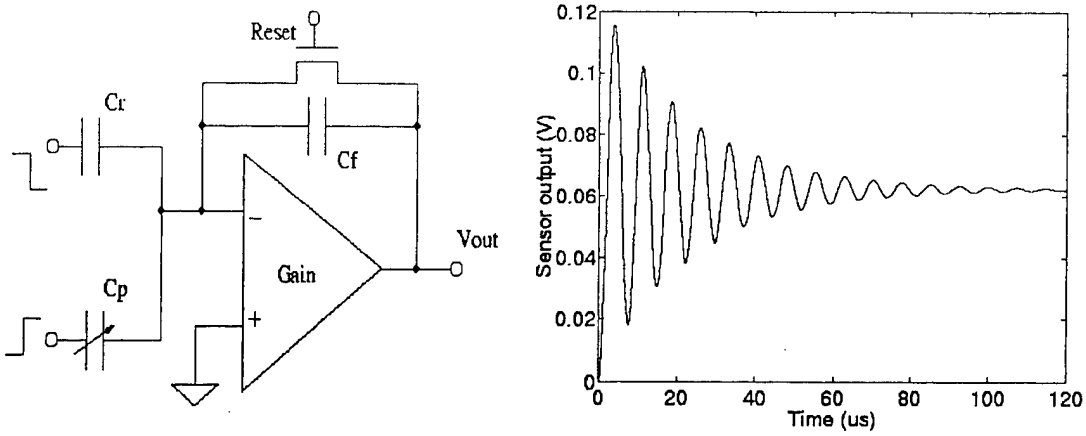
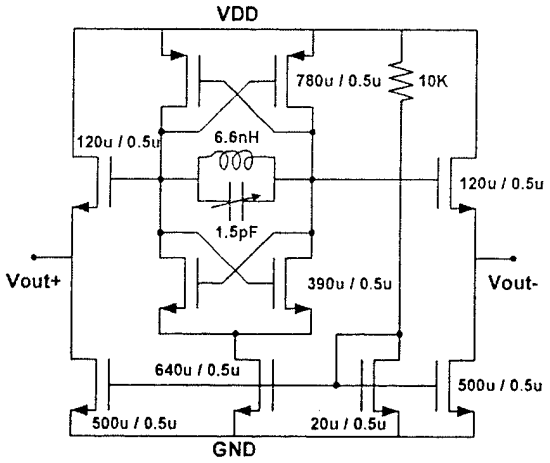
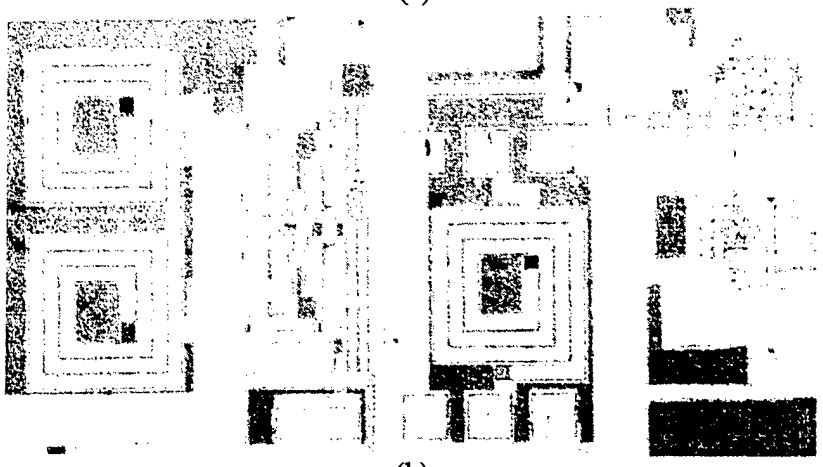


Figure 7: Schematic of a pressure sensor and response under a step increase of pressure.



(a)



(b)

Figure 8: A schematic diagram (a) and a micrograph (b) of a VCO chip realized using the MOSIS foundry process.

3.3. Design of Low Voltage Radio Frequency Switches

3.3.1. Summary

Micromachined RF switches promise to provide high performance (low on-state loss and high off-state isolation) compared with conventional IC-counterparts. In this program we have developed two types of RF switches using the CAD design tools that are either newly developed or off the shelf to efficiently design prototypes. The two types of switches offers performance levels that can be predicted by the software.

3.3.2. Type-1 switch

Switching operations are a fundamental part of many electrical, mechanical, and electromechanical applications. Products using MEMS technology are widespread in biomedical, aerospace, and communication systems. Recently, the RF MEMS have gained even more attention because of the advantages over traditional active-device-based microwave switches due to their low insertion loss, high linearity, and broad bandwidth performance. At UIUC, we proposed a new class of RF MEMS switch with low actuation voltage operation capabilities.

The advantage of using MEMS switches over FET's or PIN diodes is their low insertion loss, excellent isolation, high linearity, low power consumption and very low inter-modulation distortion. Recently, there has been tremendous progress in the development of RF MEMS switches that demonstrate less than 0.3dB insertion loss and better than 30 dB isolation from 1 to 40GHz. RF MEMS devices made by other groups include cantilever (Rockwell Group, University of Michigan) and membrane (Raytheon Group) switches. Emerging applications of RF MEMS switch technology include low-loss routing switches, phase shifters, and electrically re-configurable antenna.

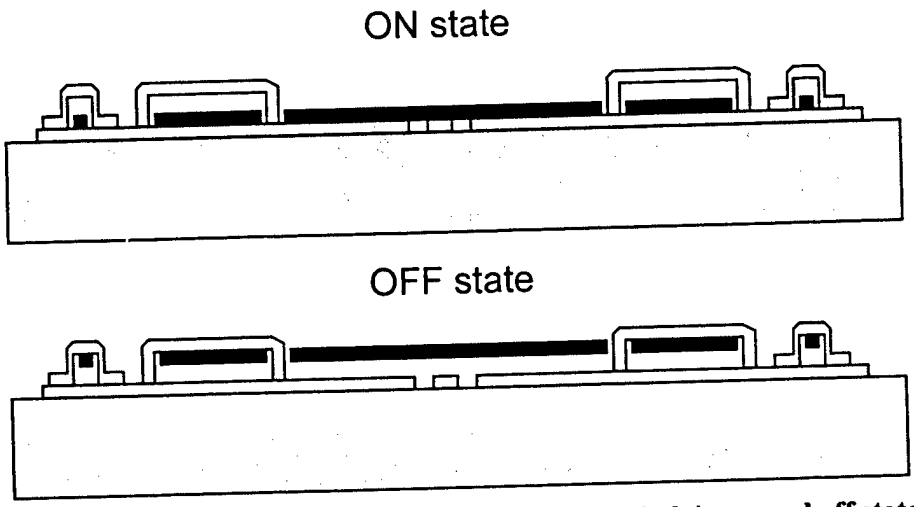


Figure 9: Schematic diagram of hinged micro RF switch in on and off states.

Low voltage operation MEMS device with an actuation voltage < 5 V and MMIC processing compatible has become an important issue for RF MEMS device development. For example, the MEMS devices with cantilever or membrane structures require high actuation voltage ranging from 25 ~ 100 Volts. The lowest voltage is that of the serpentine structure, 14 Volts. At the University of Illinois, we have developed a new class of "zero stress" RF MEMS switch that enables low voltage operation.

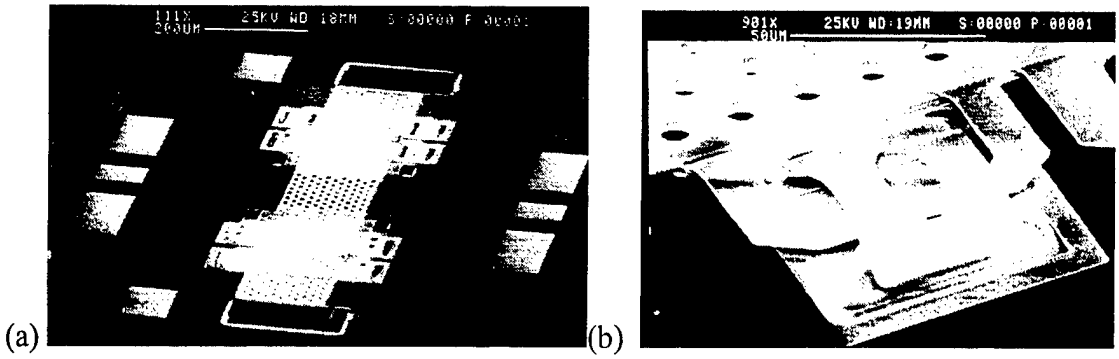


Figure 10: SEM micrographs of (a) a hinged RF switch; (b) enlarged view of the hinges.

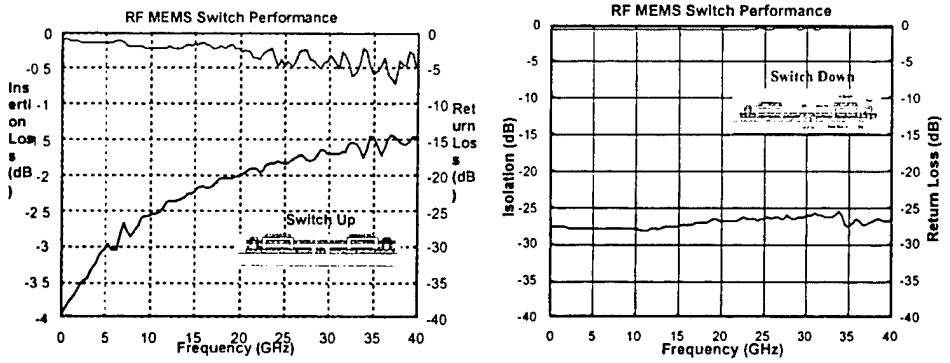


Figure 11: UIUC RF MEMS switch performance (a) insertion loss and return loss (b) isolation. The isolation is better than 27 dB throughout the entire measurement frequency range (0-40 GHz).

Utilizing a hinge structure as shown in Fig. 9, we can build a metal pad free from stress. Since the pad is not connected to any portion of the device, it can be actuated at a very low voltage (<5 V). The actuation voltage applied either on the top or bottom electrodes provide an electrostatic force to make the hinge pad move up and down. The minimum electrostatic force required by the actuation is equal to the sum of the gravitation and the air damping the hinge pad. Hence, the voltage will be much less than that for cantilever or membrane structures. Therefore, small actuation voltages for RF MEMS switches can be achieved.

SEM micrographs and test results of the switch are shown in Fig. 10 and 11. We have measured the RF performance of this MEMS switch. When the hinge is in the "up" position, we achieve an insertion loss of 0.25 dB at 20GHz and 0.5 dB at 40GHz with a return loss of –20dB at 20GHz and –15 dB at 40GHz. When the hinge is in the "down" position, we achieve isolation better than 27 dB. The switch voltage is 17 volts. We have identified barrier problems that can be

improved. Hence, we expect the switch voltage will be improved to < 5 volts, and the insertion loss will reduce to 0.25 dB and the isolation will be better than 30 dB.

3.3.3. Type-2 RF Switch

A second type RF switch was also developed for enhanced reliability. The device is shown in the figure below while under tests (Fig. 12). It consists of a top electrode that is suspended by four serpentine cantilever beams. Compared with Type-1 switch, the Type-2 switch offers higher resonant frequency, on the order and 10-50 kHz, and hence respond faster. S-parameter measurement results (S21 at on and off states, and S11 at on and off states) of the switch are illustrated in Fig. 13. The results are validated using small signal equivalent circuit models (Fig. 14).

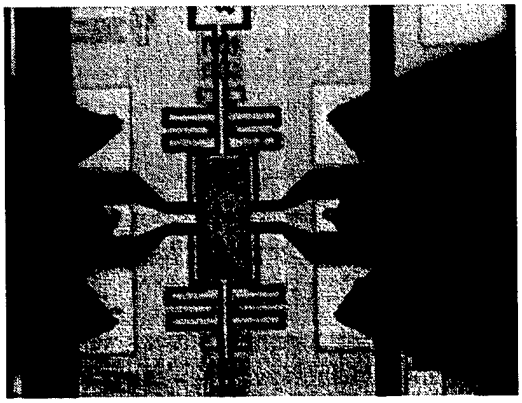


Figure 12: Micrograph of a micromachined switch under tests.

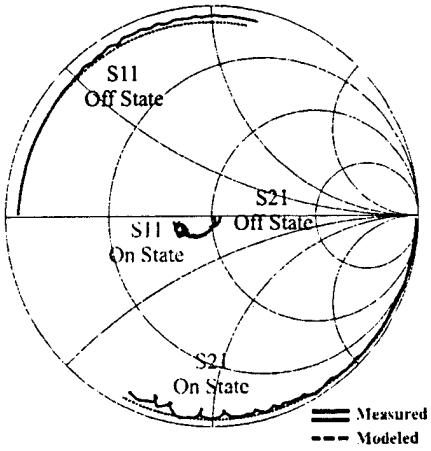


Figure 13: Measurement s-parameter performance of the micromechanical switch.

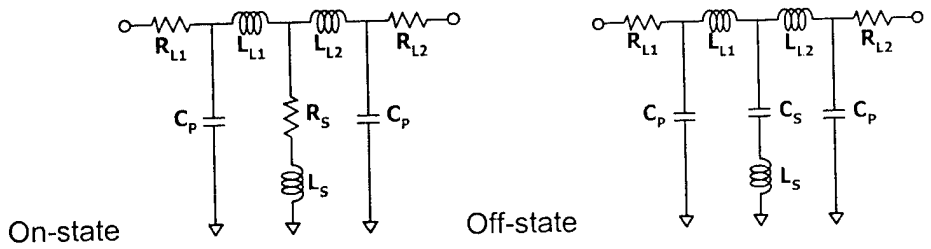


Figure 14: Simplified circuit model of the switch in on and off states.

3.4. Anisotropic Crystal Etching Simulation (ACES)

3.4.1. Continuous Cellular Automata Algorithm

A new continuous Cellular Automata (CA) model and a dynamic computational algorithm have been successfully developed and implemented. We believe that the continuous CA model represents a major advancement in the state of art of CA modeling; it is described in more detail in the next paragraph. Implementation of a dynamic CA technique has resulted in increased simulation speed and reduced memory requirements, allowing simulation to be performed on ubiquitous personal computers, rather than workstations.

In a regular CA method, states of a system are discritized; each atom is either completely intact or removed. The Continuous CA model is capable of handling *arbitrary* etch-rate ratios without any loss of simulation-system resolution and accuracy. In such a system, each cell in the system could have non-discrete states. (One non-discrete state of a cell can be viewed as its mass.) A cell can assume arbitrary states between 0 ("removed") and 1("un-touched"). During every time step, the mass value of a cell will be subtracted by the etch rate of the surface on which the cell resides. As an example, if the normalized etch rate of {110} surfaces is 0.5, mass value of cells on such surfaces will be reduced to 0.5 from 1.0 previous time step (assuming they were un-touched); the mass value would reduce to 0 in the second time step if the remains on the {110} surface. In such a case, one layer of cells on the {110} surfaces will be removed in two time steps. For a surface orientation with a desired etch rate of $E_s \in [0,1]$, assuming the time of every time step is T=1, the number of time steps (N_T) that is needed to remove a cell with a mass value of M_i on the surface equals $\mathrm{mod}(M_i / E_s T) + 1$. The equivalent etch rate of the surface, E_s', is $M_i / N_T T$.

We have developed a first PC-based 3-D etch simulator - Anisotropic Crystalline Etch Simulation (ACES) - using the continuous CA model and the dynamic method (see the figure below)). A continuous CA model allows realistic and efficient etching simulation based on complex geometric interactions among elements of the original mask. It can simulate silicon etching with different front-surface orientation in various chemical etchants, which exhibit different etch-rate ratios (Fig. 2). The program can receive 2-D mask designs in common graphics formats (including CIF, GDSII, GIF, and BMP), generate 3D profile in standard solid-modeling formats, and display results in integrated viewers based on OpenGL or VRML. The program has been offered to general public (via DARPA supported MEMS Information Clearing House) for beta-testing starting 5/1/1998.

We used two methods based on the ACES simulator to verify etch-rate diagrams (with respect to various crystalline orientations) under different etch-rate ratios. The obtained etch rate pattern is compared with experimental data to prove the validity of simulation tools. In the first method, we perform simulation of a spoke pattern, which is commonly used for directly obtaining the etch-rate diagram. It is easy to observe that simulation and experimental findings match well. Since the resolution of a lattice is limited, this method cannot achieve precise calibration of etch-rates.

Representative etch results obtained using a stochastic CA model and a continuous CA model are shown in Figure 15. The simulation results of a double rectangle mask (Figure 15a), with designated etch rate ratios of {100}:{110}:{311}:{111} = 1:0.5:0.5:0.05, are shown in Fig. 15. The resulting {111} planes based on the continuous CA model (Fig. 16b) are much more smoother compared with that based on the stochastic CA model (Fig. 16c).

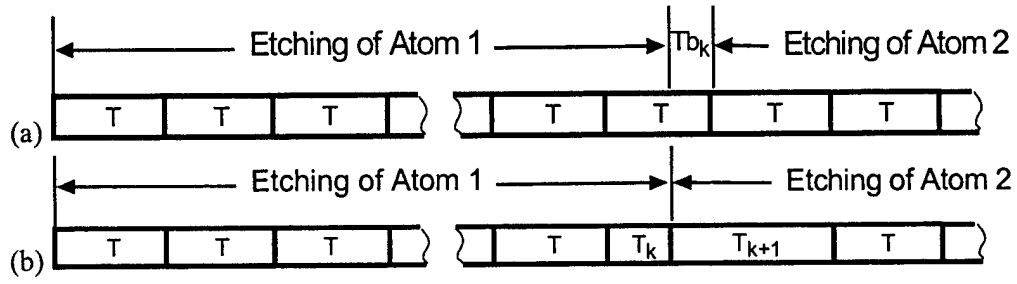


Figure 15: The schematic diagram of the continuous cellular automata algorithm. (a) Use of fractional time steps; (b) variable time steps.

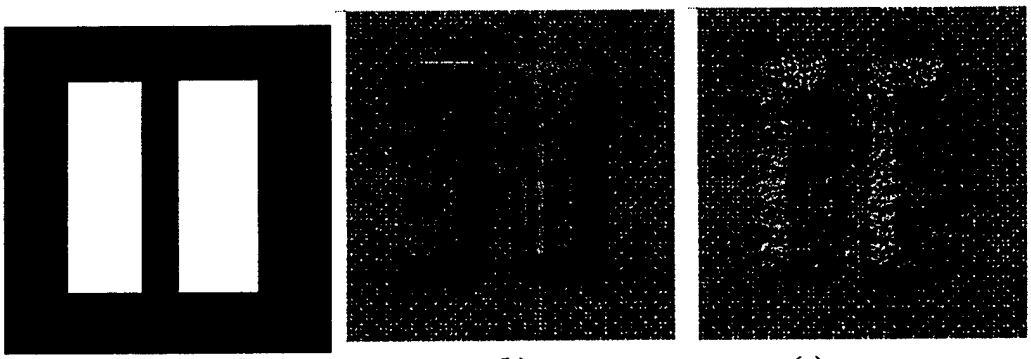


Figure 16: Different simulation results with the continuous CA model and the stochastic CA model: (a) mask, (b) etch results (top view) generated by continuous CA model, and (c) results by stochastic CA model. Sidewalls are much more smooth in (b).

The capabilities of the ACES software have been recently extended beyond simulating anisotropic etching alone. New processes are included, such as surface passivation (by thin film deposition), diffusion doping of etch-stop layers, and the dry reactive ion etching (RIE). Currently, the ACES program is able to simulate and visualize the result of a complete process flow involving several successive process steps. In the future, we plan to include more processes with increasing degree of fidelity based on the existing framework in the future. The ability to simulate and visualize complex three-dimensional micromachining processes is believed to be important for both experts and new MEMS developers.

In anisotropic etching simulation, only two possible material interfaces for the dynamic atom set exist. They are the etchant-to-silicon and the mask-to-silicon interfaces. Atoms interfacing with the mask are considered passivated and not etched. In the extended etching simulation, more materials, and therefore material interfaces, are introduced. New general materials include the passivation layer and the heavily-doped silicon. New interfaces include:

(1) The interface between silicon and thin films (e.g. deposited silicon nitride and heavily-doped etching-stop silicon layer);
(2) The interface between such thin films and etchants (liquid phase etchant in bulk etching or gas phase etchant in RIE).

Each of the interfaces constitutes an atom set. The evolution of the virtual surfaces is realized by inserting new atoms or deleting old ones from the atom set according to the physical etching characteristics. General rules for realizing the etching steps described above are summarized below:

(1) Passivation: passivation is the simplest, involving changes in the atom interface property. Interfaces between a material (denoted A) to the etchant is modified to be between A and the passivation film. The passivation film (e.g. silicon nitride) is considered completely inert in silicon etchants under current assumptions. The etch rate of wet chemicals such as EDP and KOH on the passivation layer is considered negligible. The passivation material can be removed by RIE.
(2) RIE: if a silicon atom in the dynamic atom set is interfaced with the etchant (gas phase), the atom is removed and a new one generated with the same interface type and a new depth. All structural materials including the passivation film and the doped and undoped silicon can be attacked by the gas phase etchant. Currently, the lateral undercut is considered negligible in the RIE model.
(3) Diffusion etch-stop layer formation: as the diffusion progresses beneath the surface of the original structure/etchant interface, new interfaces are generated: one (1) is between the doped silicon and the etchant, and another (2) is between the doped silicon and the underlying silicon substrate. The distance between these two interfaces indicates the thickness of the etch-stop layer. The etch rate of the wet chemical etchants on the etch stop layer is considered as zero.

To demonstrate the capabilities of the program to simulate multiple step processes, two exemplary devices are used: a buried channel and a silicon neuron probe. A method for etching channels beneath the surface of a wafer has recently been reported. First, a high-aspect-ratio trench is etched using RIE etching. After that, the surface of the wafer is passivated with a layer of silicon nitride. This nitride also covers the walls and the bottom of the trench well. The silicon nitride in the bottom of the trench is etched away using a second RIE etching, exposing silicon materials at the bottom. Next, the wafer is etched using an isotropic etchant to form buried channels. The results of ACES simulation is shown Fig. 17 following each major stage of the process: (1) RIE, (2) surface passivation and RIE, and (3) silicon wet etching (with etch rate ratios adjusted for isotropic etching).

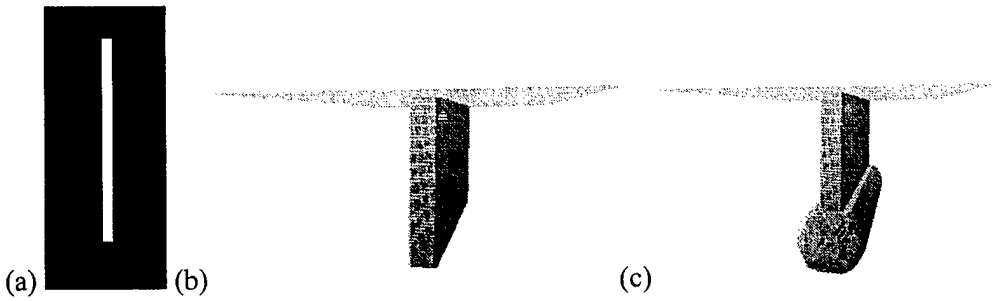


Figure 17: Simulation results of sequential etching from (a) mask layout; (b) first step reaction ion etching and surface passivation; (c) channel etching.

The software has been used by various academic and industry users. For example, a chamber for a resistojet design has been made by an engineerer at the Aerospace Corporation for DARPA micro-sat project (Fig. 18).

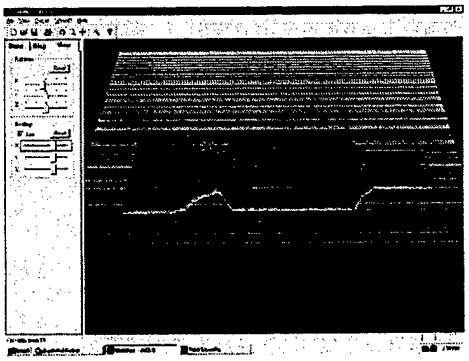


Figure 18: ACES screen-shot of a designed resistojet chamber.

3.4.2. Contribution and Impact

Before this Composite CAD program, there was no commercially available software for simulation of anisotropic etching based on complex mask shapes. The ACES software uses both advanced algorithms and has a intuitive and efficient machine-user interface. As a result, the software becomes popular among MEMS researchers. The software has been downloaded for more than 500 times by distinct users.

3.5. RF Design for Packages and Interconnects

3.5.1. Summary

We have developed several new algorithms and methods for efficient simulation of packages and interconnects of RF IC. The packaging and interconnects are important considerations in the design of RF devices.

3.5.2. Challenges for Advanced Packaging

The performance of radio frequency (RF) integrated circuits will strongly influence the versatility and portability of future wireless communication systems. With the ever increasing demands for higher bandwidth and capacity as well as reductions in size weight and cost, the need for more versatile circuits is expected to increase. Third-Generation (3G) wireless technology promises to deliver substantial improvements in size, weight, portability, power consumption and cost. It will also integrate many different functions including not only voice but also video, data which will give birth to a variety of communication devices such as personal digital assistant, automobile navigation, internet and even vending machines.

To achieve such a level of ubiquity, it is believed that a higher level of integration must be attained. Different design methodologies will need to be adopted. These methodologies will require design tools and packaging schemes that are not quite available to designers nowadays. The quest for high-bandwidth multimedia traffic will imply circuit operation at higher frequencies. Designs at these higher speeds and frequencies will necessitate a totally different set of skills in which electromagnetics and microwaves will need to be placed at the forefront.

These problems will be compounded with the need for low power and higher integration. The system on a chip (SOC) approach exhibit challenges that are rather enormous ranging from signal integrity to power dissipation constraints. Moreover, the computer-aided design (CAD) tools necessary to drive the design of such systems are not mature given the complexity and size of the problems. In deep submicron technology signal integrity problems are more serious as a result of closer proximity of the components and higher resistance of the scaled-down interconnects.

Thus new methods will have to be adopted in order to address these challenges. These methods will include fast extraction methods, efficient simulators and accurate characterization techniques. During the program period several activities in RF, microwaves and signal integrity have been undertaken in our group. These activities range from experimental characterization to the development of computational techniques for the modeling and simulation of complex networks for high-speed RF and digital applications.

3.5.3. Full-Wave Characterization of Interconnects

At high frequencies the behavior of interconnections exhibits high-order electromagnetics effects that require full-wave modeling. The integration of these full-wave techniques into existing design flow is thus an essential task. An automatic parallel extraction scheme has been developed in our group. This work is capable of handling general geometry configurations and providing highly efficient full-wave modeling.

Recently, our group completed the implementation of a full-wave design environment. The tools of this environment consist of a translator, a mesh generator, and a parallel FDTD kernel, which are integrated automatically. In all, this results in a highly efficient environment for modeling and extraction of electrical parameters used for the physical design of printed circuit boards for high-frequency applications.

The design information is exported as GDSII format file, a standard file format for transferring/archiving 2D graphical design data. The translator will parse the design file and stores the design information in an intermediate data structure. Next, the mesh generator projects the conductor information onto the Yee-like grid. The layers from GDSII files are extruded in z-direction by inserting vias and dielectric media.

The finite difference time domain (FDTD) method is employed as the full-wave simulation engine for the extraction of S-parameters due to its capability to model complicated structures. A voltage source with internal resistance is used to drive the simulation. The parallel FDTD code is automatically generated and run on a PC cluster.

The parallel FDTD simulation kernel uses MPI for communication between the nodes on the cluster. During the first iteration, each node stores the conductor information in its computational domain into the local cache in order to speedup the update. Some numerical with the commercial product "Momentum" and for large problems, our implementation showed superior performance as shown below.

TABLE 1. COMPARISON OF CPU TIME FOR MOMENTUM AND FDTD

Method	**Momentum**	**FDTD**
Domain	17666 unknowns	$120 \times 86 \times 23$
CPU Time	5.93 hours	6.9 mins

3.5.4. Three-Line Matching Network for MMIC Applications

The design and implementation of matching networks for transistor amplifiers using stub elements is a common yet important technique in microwave design. However, recent improvements in the simulation of coupled transmission lines, such as extraction of R, L, G, C, Z, and Y matrices, modal decoupling, and crosstalk modeling have allowed an extension of tuning stub theory to multiple coupled lines. Analog MMICs such as amplifiers and oscillators are typically built into stripline or coplanar waveguide structures. Substituting coupled microstrip lines as the transmission media offers potential advantages in terms of material (ground plane) and construction (via holes) savings.

During the past year, our research has focused on multiconductor transmission line (MTL) analysis and applications (Fig. 19). The central technological focus has been coupled microstrip lines. We have developed code for the analysis of given structures and the synthesis of terminations, matching networks, and amplifiers.

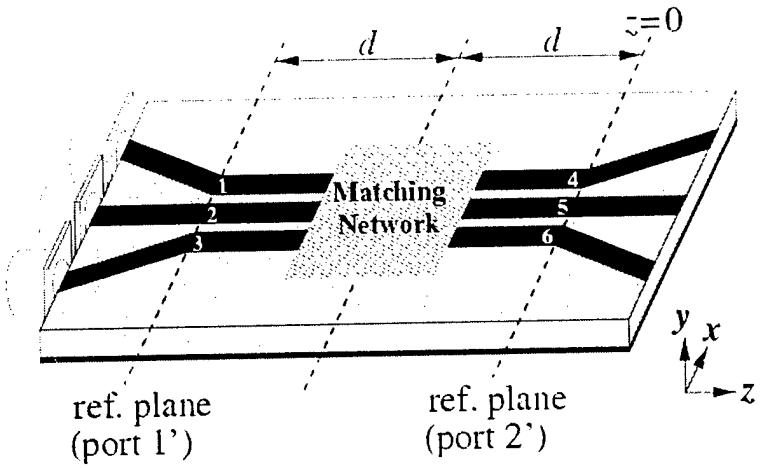


Figure 19: Multiconductor system used as matching network.

In MTL theory , we have thoroughly investigated longitudinal immittance matrix functions both mathematically and physically. Applications of this analysis include circuit modeling for two-port microwave devices based on S-parameter measurement. Particular emphasis was placed on mode delays in multimode systems, their theoetical implications and practical apllications. We have also investigated oscillation and stability theory in MTL systems.

In applications, we have synthesized, fabricated, and tested a three-line unilateral matching network on microstrip. This work was extended to a three-line coupled microstrip amplifier, complete with multiline matching networks optimized with commercial software. Filter analysis and two-tier measurement techniques were applied to this structure were necessary. Measurement calibration techniques including the multimode TRL algorithm are being incorporated into a new two-tier amplifier design method in multiline systems for improved accuracy.

3.5.5. Latency Insertion Method

The simulation of very large networks consisting of large numbers of nodes is a major problem in the computer-aided design of integrated circuits. Circuits of this size can typically require several days of CPU time on a workstation. Several investigators have introduced algorithms and numerical techniques such as the asymptotic waveform evaluation (AWE) method to approximate network transfer functions. The fundamental idea behind model-order reduction rests in the implementation of a circuit representation based on a smaller number of poles than the original network. These poles account for most of the behavior of the network over the frequency range of interest. The resulting macromodel equivalent circuits can be used in conjunction with standard circuit simulators.

Work was later introduced to reduce the number of spurious poles generated by the reduction process. This includes the complex frequency hopping techniques, and the Krylov subspace methods. More recent work on model order reduction techniques have focused on the passivity of the reduced equivalent circuits. In this study, we use a time-domain formulation that leads to the generation of update algorithms for the simulation of networks. The algorithms exhibit linear computational complexity and are scalable. Because of the time domain nature of the formulations, they can be extended to handle nonlinearities.

In our group, a finite difference formulation is used to simulate large networks. The method makes use or introduces reactive latency in all branches and nodes of a circuit to generate update algorithms for the voltage and current quantities. A criterion is established that guarantees the stability of the algorithm for specified choices of the time step. Because of its linear numerical complexity, several orders of magnitude in speedup over matrix-based methods are obtained. Nonlinear networks can also be simulated by the formulation. Several comparisons are made with standard simulators in order to evaluate the accuracy and efficiency of the algorithm. In all cases that satisfy the stability criterion, good agreements with established techniques are obtained.

The LIM method has been tested for the simulation of nonlinear networks, coupled transmission lines and large networks. In all cases, good accuracy and substantial speedup is obtained over standard simulators. Comparison of run times between SPICE and LIM for several large nonlinear networks are shown in the table below.

TABLE 2. COMPARISON OF RUN TIME FOR SPICE AND LIM

Number of Nodes	SPICE (sec)	LIM (sec)
1,000	9	0.25
10,000	334	4
15,000	701	6
20,000	1224	9
25,000	1892	11
30,000	2935	13

3.6. Design of Integrated RFIC Passives

3.6.1. Summary

Integrated passives such as capacitors and inductors are important elements of RF communication systems. It is important to develop high performance passives which can be integrated with circuits. We have developed micromachined tunable capacitors with wide tuning ranger. CAD design tools are used to produce efficient and accurate designs of the structure to reduce the time of design. The tunable capacitor has been fabricated and tested. Efforts are also made to developed integrated off-chip high-Q inductors.

3.6.2. Description of major results and approaches

Varactors based on IC technologies are widely used in current wireless communication systems. But they have generally low quality factor and can only provide limited amount of tuning range (e.g. <10%). Off-chip components often have to be used to obtain the required performance, which increases the complexity and fabrication cost of the entire system. Variable capacitors are important elements for integrated military communication systems. However, there are two major difficulties with existing MEMS integratable variable capacitors: (1) low tuning range naturally limited by the "pull in" effect and (2) large device "foot print" of devices.

Normally, the tunable capacitor is actuated by using electrostatic force, which is done by applying a DC voltage across the fixed plate and the movable plate of the tunable capacitor. Theoretically, if the tunable capacitor is used as the electrostatic actuator at the same time, the displacement of the movable plate can not exceed 1/3 of the initial gap of the capacitor to prevent the "pull-in" effect - suddenly snap in of two capacitor plates when the distance is smaller than 2/3 of the original value. This effect brings an upper limit to the tuning range, 1.5:1. This tuning range is not adequate to cover the wide bandwidth requirement for various military wireless communication systems. In addition, due to the relatively large gap between the capacitor plates, the area of the capacitor must be large to accommodate adequate capacitance, as the capacitance is expressed as

$$C = \frac{\varepsilon_r A}{d},$$

where A is the overlap area, d is the spacing, and ε_r is the dielectric constant (typically air).

A new design of parallel plate capacitor has been conceived and developed through our effort. According to this design, the tunable capacitor and the actuating capacitor are separate (Fig. 20). The DC driving voltage is applied on the actuating capacitor. The initial gap between the two plates of the tunable capacitor is 1μm, whereas the initial gap between the two plates of the actuating capacitor is 2 μm. So the maximum displacement of the movable plate can reach more than 0.67μm (1/3 or 2 μm) before the "pull-in" effect occurs. This corresponds to a 3:1 tuning range of the tunable capacitor. If the initial separation at the capacitor can be further reduced reliably using micromachining processes, the tuning ratio can increase dramatically. In regular variable capacitor with parallel plate configuration, the distance between the two plates is usually large (e.g. 2-3 μm) to allow maximum movement. However, the large distance reduces the capacitance value. For routine required capacitor (e.g. 2 pF), an effective area of 1x1 mm^2 is needed, straining the already limited real estate on chip. In the new design, the separation distance is much smaller; therefore the required area for a given capacitance value is reduced accordingly.

The overall benefits of this novel design are (1) much increased tuning range; (2) reduction of the area requirement of tunable capacitors; (3) reduction of requisite range of electrostatic voltage. A driving voltage less than 10V or even smaller can be achieved by carefully controlling the thickness of the support beams.

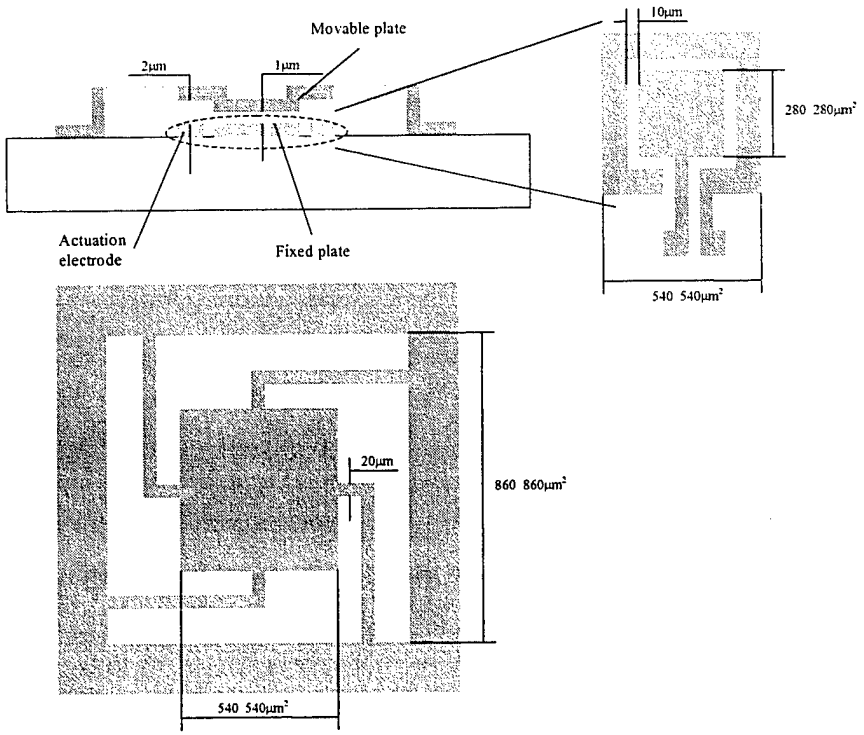


Figure 20: Schematic diagram of a wide tuning range tunable capacitor.

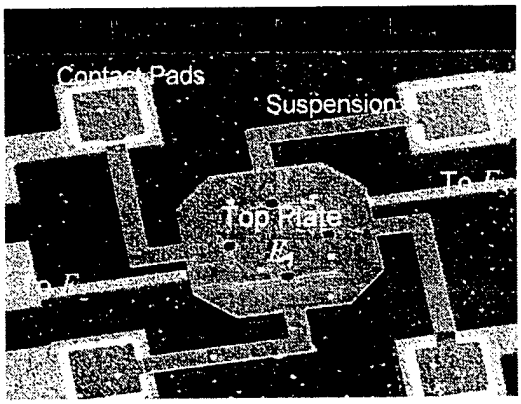


Figure 21: An SEM micrograph of the developed tunable capacitor.

In order to efficiently design the capacitor we have actively used electromechanical simulation tools such as the MEMCAD, high-frequency simulation tools such as the HP ADS (Advanced Design Systems) (Fig. 21 and Fig. 22). A three-dimensional model of the tunable capacitor is shown in the figure below. The resulting change of capacitance as a function of the input voltage is illustrated in the next diagram (Fig. 23).

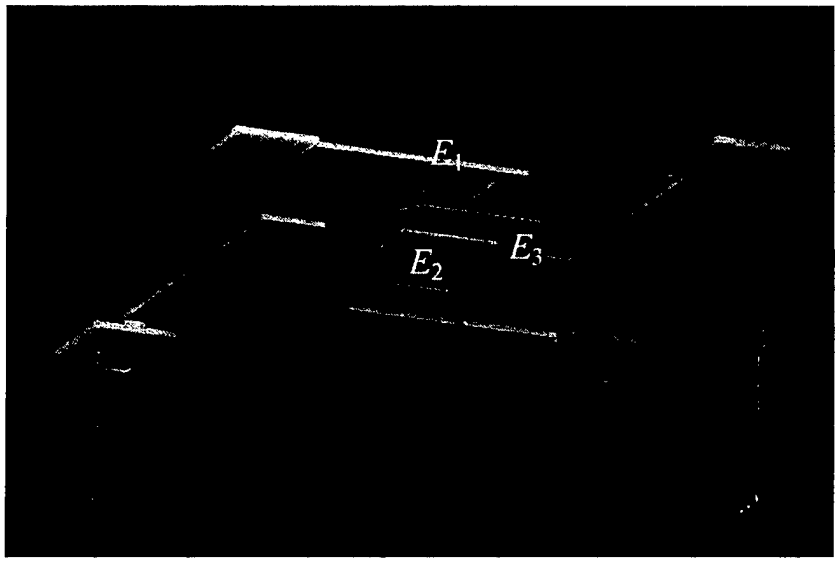


Figure 22: Three-dimensional model of the tunable capacitor.

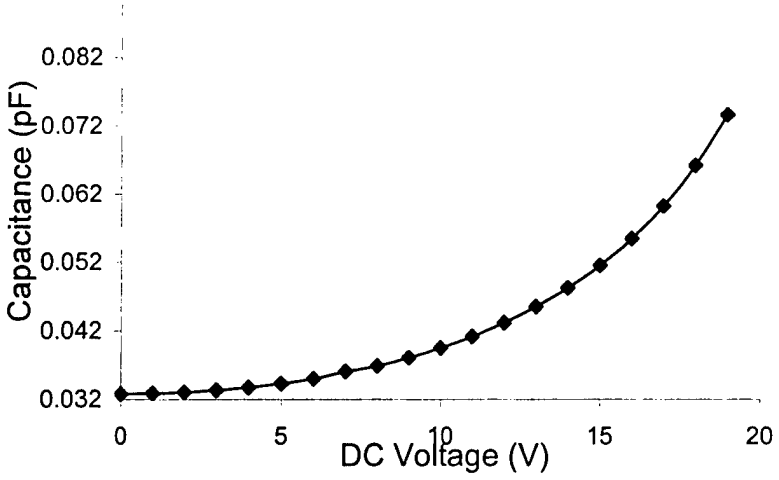


Figure 23: C-V curve obtained by MEMCAD simulation showing a tuning range of 90.5%.

In addition to the development of capacitors we have invented new designs and fabrication processes for realizing high performance inductors. Traditional planar inductors such as the ones shown in the VCO circuit are widely used. However, such inductors suffer from two major challenges. First, the inductors, when located on top of lossy substrates such as silicon, experiences leakage current loss and a reduction of quality factor. Secondly, the inductors occupy large footprint in order to realize large inductance value.

We developed a vertical planar inductor as illustrated in the diagram below. The vertical inductor solves two of the most important challenges. First, the substrate loss is reduced as the current-carrying coils are separated from the substrate, hence reducing the leakage current. Secondly, the footprint of such device is significantly reduced from the conventional counterparts as the inductors are lifted away from the substrate. The fabrication process used to develop the vertical

inductor is called the plastic deformation magnetic assembly (PDMA) process (Fig. 24). Details of the process can be found in related publications.

The transmission parameter measurement results (s11) are shown in Fig. 25. The s-parameter curve of the vertical inductor on a silicon substrate closely resembles the ideal inductor. The curve for the device on a silicon substrate, on the other hand, shows significant loss. The loss of the vertical inductor is low, comparable to the curve of a similar device located on a low-loss, glass substrate.

3.6.3. Lessons learned

The validation of advanced simulation codes for RF front-ends demands expertise in RF design and measurements. The research teaming is very useful in terms of providing opportunities of collaborations between faculty members in the area of RF measurement (Prof. Jose Schutt-aine), RF design (Prof. Milton Feng), and device developers (Prof. Liu). Through this program we have established measurement equipment, testing protocols, and design guidelines. However, the testing is much more difficult than previously anticipated. We have spent a lot more time than anticipated to build the measurement experience among students. In future DARPA programs of similar nature, it is important to provide dedicated funding and students for RF testing.

4. Plans for Future Work

Although the program was successfully finished and many of the projected milestones have been met, we have met with some difficulties that were not expected at the beginning of the program. For example, the efforts spent on testing and validation was much more than initial projection. As a result, we did not finish many expected device devices and tests, for example dynamic testings of the switch and capacitor. However, the testing setup has been established near the end of the program and these allow us to conduct follow up tests.

We plan to further complete efforts to commercialize the software algorithms. A start-up company has been established by the faculty members in the CCEM (Center for Computational Electromagnetics) and some of the students who have recently graduated. The algorithms and codes will be commercialized through the company. Prof. Schutt-aine has also established a start up company to design advanced optoelectronics. The EM simulation algorithms for packages and interconnects will be utilized and commercialized. The iSIMS software codes developed by Prof. Kang is being further developed at the University of California at Santa Cruz.

We are also interested in furthering our efforts of developing integrated front-end systems containing various components that have been developed through this effort. Such work would require collaboration of various faculty members including Prof. Feng and Liu.

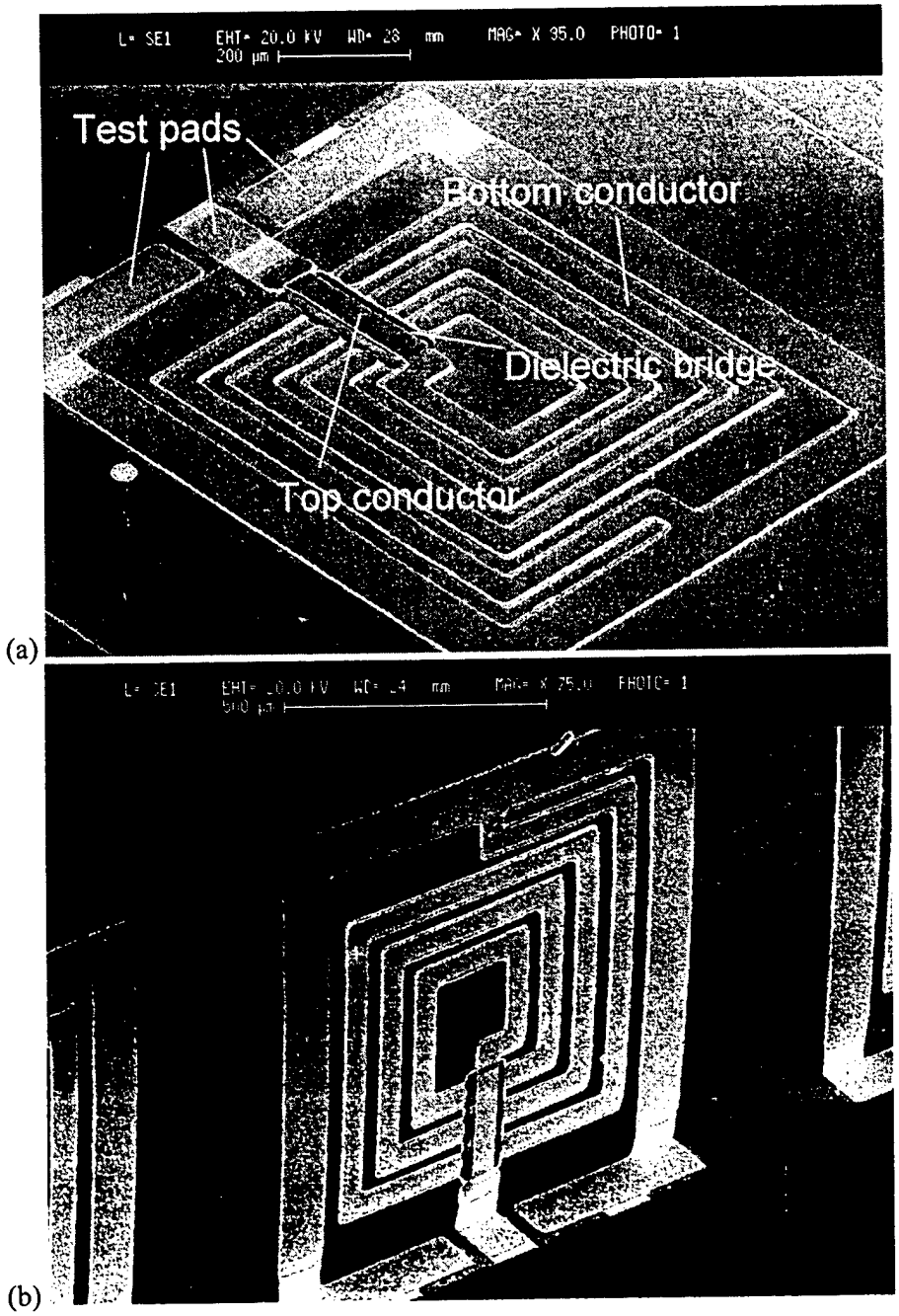


Figure 24: SEM micrograph of vertical inductor. (a) Before three-dimensional assembly; (b) After assembly is completed.

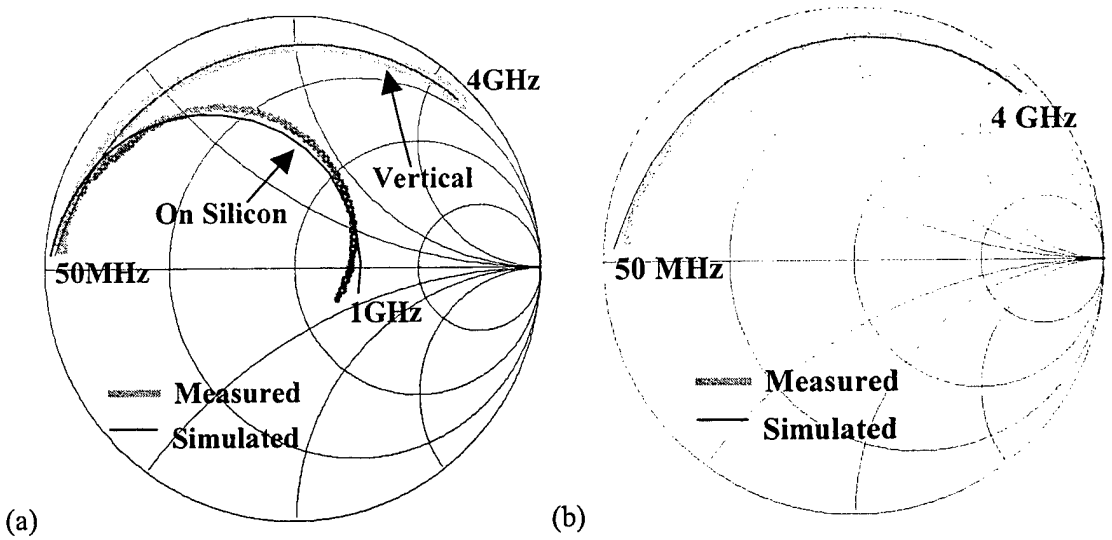


Figure 25: S-parameter analysis of the vertical inductor in contrast to inductors on glass and silicon substrates.

5. List of Publications

1. J. Chen, K. Coperich, S-M Kang, and J. Schutt-Aine, Parameter Extraction for a Microwave Micromachined Switch, MSM'99, April 19-21, Puerto Rico.
2. J. Chen and S-M Kang, A Mixed Frequency-Time Approach for Quasi-periodic Steady-State Simulation of Multi-level Modeled Circuits, ISCAS'99, May 31 -June 2, Orlando, FL.
3. M. Lu, J. Wang, E. Michielssen, A. Ergin, and B. Shanker, "Diagonal translation operators for two-dimensional transient wave fields," Journal of Computational Physics, 1999, submitted.
4. M. Lu, E. Michielssen, P. Mayes, and P. Ingerson, "A dual mode log-periodic cavity-backed slot antenna," International IEEE-AP Symposium, Orlando, FL, June 1999.
5. M. Lu, J. Wang, A. Ergin, and E. Michielssen, "A diagonal translation operator for the fast evaluation of two-dimensional wave fields," International IEEE-AP Symposium, Orlando, FL, June 1999.
6. J. Wang, M. Lu, and E. Michielssen, "Acceleration of two-dimensional time domain integral equation solvers using a Hilbert transform," International IEEE-AP Symposium, Orlando, FL, June 1999.
7. J. Wang, B. Shanker, M. Lu, and E. Michielssen, "Exact absorbing boundary conditions for 2D FDTD simulations based on multilevel plane wave time domain algorithms," International URSI Symposium, Orlando, FL, June 1999, accepted.
8. N. Gres, B. Shanker, and E. Michielssen, "Fast analysis of transient electromagnetic scattering from inhomogeneous penetrable bodies using the multilevel plane wave time domain algorithm," SES meeting, October 26-27, Austin, TX, accepted.
9. M. Feng and S. C. Shen, "A novel MEMS RF switch with low actuation voltage," U.S. patent pending, Serial no. 09/326,771, June 4, 1999.
10. S. C. Shen and M. Feng, "Low Actuation Voltage RF MEMS Switches With Signal Frequencies From 0.25GHz to 40GHz," pp. 689-692, IEEE 1999 International Electron Device Meeting, Washington D.C., Dec.5-8, 1999.

11. M. Feng and S.C. Shen, " Optical Controlled Low Actuation Voltage Microelectromechanical Switches ," U.S. patent file # 1201.63890, June 20, 2000.
12. S. C. Shen, David Caruth, and M. Feng, "Broadband Low Actuation Voltage RF MEMS," To be presented at 2000 IEEE GaAs IC Symposium in September, 2000.
13. Jun Zou, Chang Liu, "Wide tuning range MEMS tunable capacitor", Device Research Conference (DRC), Denver, CO.
14. Jun Zou, Chang Liu, "Design of a wide tuning-range MEMS varactor", First IEEE Electro/Information Technology, Conference, June 8-11, Chicago, IL, 2000.
15. Zhenjun Zhu, Chang Liu, "Micromachining process simulation using a continuous cellular automata method," J. MEMS, Vol. 9, No. 2, pp. 252-61, 2000
16. Z. Zhu and C. Liu, "Simulation of anisotropic crystalline etching using a continuous cellular automata algorithm," Journal Computer Modeling for Engineering and Science, Vol. 1, No. 1, pp. 11-19, 2000.
17. Jun Zou, Chang Liu, Jinghong Chen, Steve Kang and Jose Schutt-Aine, "Development of a Wide Tuning Range MEMS Tunable Capacitor for Wireless Communication Systems", IEDM, San Francisco, 2000
18. Jun Zou, Jack Chen, Chang Liu, "Plastic deformation magnetic assembly - design and methodology", Journal of MEMS, accepted, January 2000.
19. F. Liu, J. Schutt-Aine and J. Chen, "Full Wave Analysis and Modeling of Multiconductor Transmission Lines," submitted to IEEE Trans. Microwave Theory Tech., February 2000.
20. F. Liu and J. E. Schutt-Aine, S. Velamparambil, W. C. Chew, "Application of Parallel Computation to Full-Wave Interconnect Extraction," Proceedings of IEEE Workshop on Signal Propagation in Interconnects, SPIE, Titisee-Neustadt, Germany, May 1999.
21. Feng Liu, J. E. Schutt-Aine and Ji Chen, "Full Wave Analysis of Transmission Lines via 2D-FDTD and Signal-Processing Techniques," 1999 IEEE-APS, Orlando, FL.
22. S. V. Velamparambil, J. E. Schutt-Aine, J. G. Nickel, J. M. Song, and W. C. Chew, "Solving large scale electromagnetic problems using a Linux cluster and parallel MLFMA", 1999 IEEE-APS, Orlando, FL, July 1999.
23. J. G. Nickel and J. Schutt-Aine, "The Effects of Quasi-TEM Modal Dispersion on Longitudinal Immitance Matrix Functions of Lossless, Symmetric Coupled Microstrip Systems," EM Lab Technical Report No. 00-1, February 2000.
24. J. G. Nickel and J. E. Schutt-Aine, "Quasi-TEM modal dispersion effects on immittance matrices of lossless, symmetric, coupled-microstrip systems", submitted to [7] J. G. Nickel and J. E. Schutt-Aine, "Narrowband Matching Networks for Quasi-TEM Coupled Microstrip Lines," submitted for publication to IEEE Trans. Microwave Theory Tech.
25. W. T. Beyene and J. E. Schutt-Aine, "Accurate Frequency-Domain Modeling and Efficient Circuit Simulation of High-Speed Package Interconnects," IEEE Trans. Microwave Theory Tech., vol. MTT-45, pp.1941-1947, October 1997.
26. J. Schutt-Aine, "Latency Insertion Method for the Fast Simulation of Interconnection Networks," Proceedings of the 8th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP), San Diego, CA, October 1999.
27. J. E. Schutt-Aine, "Latency Insertion Method for the Fast Transient Simulation of Large Networks," to be published in IEEE Trans. Circuit Syst. I.

MISSION
OF
AFRL/INFORMATION DIRECTORATE (IF)

The advancement and application of Information Systems Science and Technology to meet Air Force unique requirements for Information Dominance and its transition to aerospace systems to meet Air Force needs.